REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow.

A key feature of the semiconductor integrated circuit wafer scale structure claimed as Applicant's invention is the utilization of a unitary, substantially planar, solid glass sheet having substantially the same size as the wafer substrate and having a plurality of prefabricated holes formed therethrough. That is, the wafer-sized solid glass sheet has a pattern of prefabricated holes formed in it prior to attachment of the solid glass sheet to the semiconductor wafer substrate. Affixation of the solid glass sheet to the wafer substrate aligns the pattern of prefabricated holes in the solid glass sheet with associated die bond pads formed on each of the individual integrated circuit die that are formed on the semiconductor wafer. This facilitates the formation of a solder ball bond pad structure that extends from the upper surface of the solid glass sheet through the solid glass sheet and through adhesive material disposed between the solid glass sheet and the wafer substrate to provide an electrical connection between a conductive solder ball formed on the solder ball bond pad structure and an associated die bond pad formed on the integrated circuit die.

Applicant submits that nothing in the prior art either teaches or suggests such a unitary, substantially planar solid glass sheet having a plurality of prefabricated holes formed therethrough in a wafer-scale integrated circuit structure.

In the February 19, 2002, Office Action in this application, the Examiner rejected claim 52 under 35 U.S.C. §112, second paragraph, as being indefinite. As indicated above, claim 52 has been cancelled.

The Examiner rejected claims 49-58 under 35 U.S.C. §103(a) as being unpatentable over the Kata et al. in view of Lin, Tsukamoto, Igarashi et al. and Feldner et al.

As stated above, Applicant believes that the element recited in each of Applicant's new [illegible] substantially planar solid glass sheet

holes formed therethrough is a feature neither taught nor suggested by any of the references cited by the Examiner, whether considered individually or in combination.

Aside from the fact that the reference combination cited by the Examiner neither teaches nor suggests a key feature of Applicant's claimed invention, it is submitted that the analysis of the Kata et al./Lin/Tsukamoto/Igarashi et al./Feldner et al. reference combination provided by the Examiner in the Office Action does not lead to the invention defined by Applicant's new independent claims 59, 66 and 67.

More specifically, each of Applicant's new independent claims defines a semiconductor wafer substrate that includes a plurality of semiconductor integrated circuit die formed on an upper surface of the wafer substrate. Each individual semiconductor integrated circuit die includes a plurality of conductive die bond pads formed on an upper surface of the integrated circuit die. The independent claims then also go on to recite that the claimed wafer-scale structure includes a unitary, substantially planar solid glass sheet having substantially the same size as the wafer substrate and having a plurality of prefabricated holes formed therethrough from an upper surface of the solid glass sheet to a lower surface of the solid glass sheet. Each prefabricated hole formed in the solid glass sheet has an associate conductive solder ball bond pad formed on an upper surface of the solid glass sheet in proximity to the prefabricated hole. Adhesive material is disposed between the upper surface of the wafer substrate and the lower surface of the solid glass sheet to affix the solid glass sheet to the wafer substrate such that each prefabricated hole in the solid glass sheet is aligned with an associated die bond pad formed on integrated circuit die.

The Examiner refers to the Kata et al. reference as showing a wafer scale device with the wafer connected through film 64 to bumps 70. The film 64 in the Kata et al. structure is recited in the specification of the '304 patent as being a polyimide film applied to have a thickness of 20 micrometers or smaller. The Kata et al. structure also includes a passivating film 12 formed between the covering coating film 64 and the wafer 10. In addition to failing to disclose the feature discussed above, the Kata et al. reference also fails to disclose an interconnect structure [illegible] Applicant's new independent claims.

the interposer board attached to a PC board with a layer of adhesive 36, but does not show a similar attachment between semiconductor die 12 and rigid interposer 22. That is, the Examiner is now referring to a reference that is devoid of any discussion of a wafer level semiconductor integrated circuit structure having a wafer-scale glass sheet affixed to a semiconductor wafer utilizing an adhesive. That is, The Examiner is relying on structure that is not similar to that claimed by Applicant's invention, in that there is no adhesive material between the interposer board 22 and semiconductor chip 12, to obviate claims that are directed to a wafer scale structure.

The Examiner then cites the Tsukamoto et al. reference as teaching an "intermediate substrate" ceramic glass plate 3 in a flip-chip structure. However, the ceramic 3 is not affixed to semiconductor wafer utilizing an adhesive material.

The Igarashi et al. reference is cited as teaching use of polyimide to bond a die to an intermediate sheet. However, the polyimide resin in die-size structure disclosed by Igarashi et al. "encapsulates" the die and is thus not comparable to the wafer-scale layer of adhesive material recited in applicant's claims.

The Feldner et al. reference is cited by the Examiner as showing particular features of a chip scale device. However, Applicant again submits that the claimed invention is directed to a wafer scale device.

In view of the above, applicant respectfully submits that it is difficult to comprehend how individual features of five different chip scale structures disclosed in five different references can be combined to arrive at Applicant's claimed wafer scale structure, particularly when the five-reference combination cited by the Examiner is totally lacking in disclosure of key features of the claimed invention.

Applicant also submits that the reference combination cited by the Examiner is improper as lacking proper motivation to combine the references in the way suggested by the Examiner.

It has been held by the Federal Courts on numerous occasions that a combination of reference teachings is improper unless the prior art suggests such a combination. See, for example, *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). Although a structure can

modification. As discussed above, applicant submits that the five references cited by the Examiner cannot be combined to arrive at the claimed invention, much less provide the motivation to do so. See, for example, *In re Laskowski*, 871 F.2d 115, 110 USPQ.2d 1397 (Fed.Cir. 1989). The inquiry is not whether each element existed in the prior art, but whether the prior art made obvious the invention as a whole for which patentability is claimed. See, for example, *Hartness International, Inc. v. Simplimatic Engineering Company*, 819 F.2d 1100, 2 USPQ.2d 1826 (Fed.Cir. 1987). To establish a prima facie case of obviousness based on a combination of the content of various references, there must be some teaching, suggestion or motivation in the prior art to make the specific combination that was claimed by the Applicant. See, for example, *In re Dance*, 160 F.3d 1339, 48 USPQ.2d 1635 (Fed.Cir 1998). When relying on numerous references or a modification of prior art, it is incumbent upon the Examiner to identify some suggestion to combine references or to make the modification. Other than general comments, the Examiner does not identify the text of the cited references that would suggest the specific combination claimed by applicants. See, for example, *In re Mayne*, 104 F.3d 1339, 41 USPQ.2d 1451 (Fed.Cir. 1997). The claimed invention must be considered by the Examiner as a whole, and multiple cited prior art references must suggest the desirability of being combined, and the references must be viewed without the benefit of hindsight afforded by the patent application disclosure. See, for example, *In re Paulson*, 30 F.3d 1475, 31 USPQ.2d 1671 (Fed.Cir. 1994). To reject a claim for obviousness in view of a combination of prior art references, a showing of a suggestion, teaching or motivation must be clear and particular. See, for example, *In re Dembiczak*, 175 F.3d 994, 50 USPQ.2d 1614 (Fed.Cir. 1999).

In view of the above, Applicant respectfully submits that the Examiner's rejection of Applicant's claims based on the five reference combination cited by the Examiner is absent the clear and particular showing of a suggestion, teaching or motivation to combine the references and, that the combination of the references is arrived at only with the improper hindsight utilization of Applicant's disclosure.

For the reasons set forth above, Applicant is of the good faith belief that all claims now present in this application are in compliance with all requirements of 35 U.S.C. §112 and patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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